Simulation Studies of Shunt Passive Harmonic Filters: Six Pulse Rectifier Load – Power Factor Improvement and Harmonic Control

Seema P. Diwan, Dr. H. P. Inamdar, and Dr. A. P. Vaidya
Walchand College of Engineering, Electrical Department, Sangli, India
Email: seemapdiwan@gmail.com

***Abstract*— This paper presents a study of harmonic filters design procedure to minimize harmonic distortion caused by a harmonic source such as drives. The non – linear load considered in this paper is six pulse rectifier load. Design and simulation procedure with respect to this load is explained in details. Several types of shunt harmonic filters are presented. Shunt filters are effective in minimizing voltage distortion caused by nonlinear loads in industrial power systems. Different alternatives of filter design should be considered before making the final decision on filter configuration. Among the criteria used for performance evaluation are current, and voltage ratings of each of the filter components. The design and performance of single-tuned and high-pass filters and the methodology used for the analysis will be discussed.**

The major objectives in this study are to use shunt passive filters for following -(i) to improve the power factor, (ii) to reduce current and voltage distortion to standard limits, and (iii) to reduce resonance problems, if any.

***Index Terms*— Harmonics, passive shunt filters, single tuned filter, high pass filter, filter rating.**

I.INTRODUCTION

In an ideal power system, electrical energy is supplied at a constant frequency and at a specified voltage level of constant magnitude with sinusoidal wave shape. However, in practice, none of these conditions is fulfilled to the fullest extent, due to the presence of voltage and current harmonics of multiple orders. These harmonics may be caused by nonlinear loads like controlled rectifiers and inverters, luminous discharge lighting, magnetizing current drawn by transformers or phase belt, chording, skewing, slotting and air gap irregularities in a rotating electrical machine [1]. The harmonics present in the electrical source cause many ill-effects such as reduction in power generation, transmission and utilization efficiency, resonance effects, malfunctioning of protective relays and interference with communication equipment[2-4]. To overcome such problems, harmonic mitigation is becoming important for both utilities and customers. Filtering harmonics using passive filter is one of the earliest methods used to address harmonic mitigation issues. Passive filters have been used in power system to mitigate harmonic distortions [5] primarily due to their low cost.

Most distribution systems require reactive power compensation to improve the power factor, save demand charges, or to release additional active power from existing equipment or for voltage support, i.e., the reactive power support required to arrest the voltage drop on loss of a plant generator. The nonlinear loads are increasing, i.e., pulp and paper mill distribution systems invariably have adjustable-speed drive(ASD) systems [2], which may form a considerable percentage of overall plant load. When power capacitors are used for reactive power compensation, it becomes necessary to turn them in to filters to escape harmonic resonance problems with one of the load-generated harmonics It is not uncommon to apply passive filters in the megavar range and filters totaling some tens of megavars in a large installation may be required.The main contribution of this paper is to presents an analysis and simulation of application of shunt harmonic filters. The study procedure adopted in this paper is outlined as follows:

1. Problem definition and Simulation of a system with non linear loads.
2. Design of Shunt Passive Filter(s) to provide reactive power compensation and minimize TDD at PCC.
3. Study different aspects of design of shunt passive filter i.e. capacitor bank current and voltage loading, outage conditions of filters and resonance etc.
4. Comparison of analytical solution of the filter design and results obtained from the simulation.

II.SINGLE TUNED FILTER

The most common type of shunt passive filters used in harmonic mitigation is the single tuned filter (STF) which is either a low pass or band pass filter. This type of filter is simplest to design and the least expensive to implement [3]. The configuration of a single tuned filter is depicted in Fig.1.

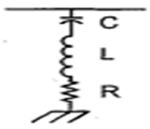


Fig.1 Single Tuned Filter

DOI: 01.IJEPE.02.01.25

In an ST filter, the inductive and capacitive reactance at the tuned frequency should be equal [3][4][5].

$$Z = R + j\omega_n L + \frac{1}{j\omega_n C} = R \quad (1)$$

$$\omega_n = \frac{1}{\sqrt{L\,C}} \quad (2)$$

If X_0 is the reactance of the capacitor or filter reactor at its tuned frequency

$$X_0 = \omega_n L = \frac{1}{C\omega_n} = \sqrt{\frac{L}{C}} \quad (3)$$

Q gives the quality factor of the tuning reactor.

$$Q = \frac{X_0}{R} = \frac{\sqrt{\frac{L}{C}}}{R} \quad (4)$$

It determines the sharpness of tuning. The passband is bounded by frequencies at which

$$|Z_f| = \sqrt{2}R \quad (5)$$

$$\delta = \frac{\omega - \omega_n}{\omega_n} \quad (6)$$

The sharpness of tuning is dependent on R as well as X_0 and reducing these can reduce the impedance of filter at resonant frequency.

III.DAMPED OR HIGH-PASS FILTER

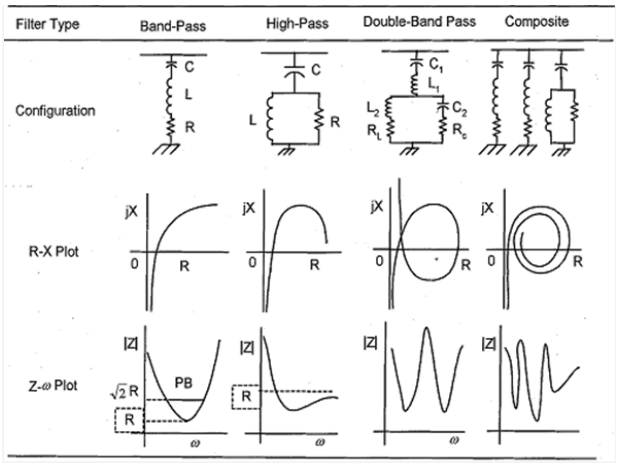
High pass filter provides a low impedance for a wide spectrum of harmonics without the need for subdivision of parallel branches with increased switching and maintenance problems [3].The sharpness of tuning in the second order high-pass filter is the reciprocal of ST filters [4][5]

$$Q = \frac{R}{\left(\frac{L}{C}\right)} = \frac{R}{X_L} = \frac{R}{X_C} \quad (7)$$

The behavior of damped filter has been described with the help of two parameters. [4][5]

$$f_0 = \frac{1}{2\pi CR} \quad (8)$$

$$m = \frac{L}{R^2 C} \quad (9)$$



Typical values of m are in the range of 0.5 and 2. For a given capacitance these parameters are decided to achieve an approximately high admittance over the required frequency range.

Impedance of filter as a function of harmonic frequency is given as

$$Z = \frac{R\,n^2 X_L^2}{R^2 + n^2 L^2 \omega^2} + \frac{jR^2\omega Ln}{R^2 + n^2 L^2 \omega^2} - \frac{j}{\omega Cn} \quad (10)$$

Fig. 2 shows various types of filters and their $Z - \omega$ plots.

IV.EVALUATION OF FILTER DUTY REQUIREMENTS

Evaluation of filter duty requirements typically involves capacitor bank duties. These duties include peak voltage, current, kVAr produced, and rms voltage. IEEE Standard 18-1992, *IEEE Standard for Shunt Power Capacitors*, is used as the limiting standard to evaluate these duties. Computations of the duties are divided into three steps, i.e., computation for fundamental duties, harmonic duties, and rms current and peak voltage duties and evaluation of capacitor loading limits[4].

1) Computation of fundamental duty requirements

The computation is as follows:

The effective reactance of the combined capacitor and reactor at the fundamental frequency is [6]

$$X_{eff} = |X_C - X_L| \quad (11)$$

The fundamental frequency current for a wye-connected harmonic filter is calculated by Equation [6]

$$I_f(1) = \frac{V_S}{X_C - X_L} \quad (12)$$

where

V_S is the maximum system operating voltage, phase to neutral, X_C is the capacitive reactance at fundamental frequency, X_L is the inductive reactance at fundamental frequency. The nominal capacitor current based on rated voltage and rated kVAr is calculated to be [6][7][8].

$$I_{nom} = \frac{Q_{cap}(kVAr)}{\sqrt{3}\,V_{rated}\,(kV)} \quad (13)$$

The fundamental frequency voltage across capacitor is [6]

$$V_C(1) = I_f(1)\,X_C \quad (14)$$

This is the nominal fundamental voltage across the capacitor. It should be adjusted for any contingency conditions (maximum system voltage), and it should be less than 110 percent of the capacitor rated voltage [6].

Fundamental frequency per phase reactive power of capacitor is given as [6]

$$kVAr(1) = V_C(1)I_f(1) \quad (15)$$

2) Computation of harmonic duty requirements

The computation is as follows:

The maximum harmonic current is the sum of the harmonic current produced by the load and that contributed from the utility side.

The harmonic current is given as [4]

$$I_{rms} = (I_{f_1}^2 + I_{f_3}^2 + I_{f_5}^2 + I_{f_7}^2 + \ldots\ldots)^{1/2}\text{A} \quad (16)$$

DOI: 01.IJEPE.02.01.25

Assuming the harmonic and fundamental components add together, the maximum peak voltage across the capacitor is

$$V_{C\,peak} = [V_C(1) + V_C(h)] \quad (17)$$

where $V_C(h) = \sum_{h=2} I(h)\left(\frac{X_C}{h}\right)$

The rms voltage across the capacitor is [4]

$$V_{C\,rms} = \sqrt{[V_C(1)^2 + V_C(h)^2]} \quad (18)$$

Although IEEE Std 1036-1992 allows for continuous operation of the capacitor at a voltage 110% above the rms-rated voltage and 120% above the peak of the rated voltage, these margins should be reserved for contingency operation [6]. Consequently, the design for the harmonic filter rates the capacitor voltage at 100% of the most severe operating condition.Based on the line-to-line rated voltage of the harmonic filter capacitor and the impedance of the harmonic filter capacitor bank, the rated three-phase Mvar of the capacitor bank is [4]

$$Q_{rated} = \frac{(\sqrt{3}\,V_r)^2}{X_C} \quad (19)$$

where

Q_{rated} is the three-phase rating of capacitor bank (Mvar), X_C is the impedance of capacitor bank per phase (&!).3) Evaluation of capacitor rating limits.The duties (peak voltage, rms voltage and current, and kvar produced) for the proposed filter capacitor are compared to the various IEEE standard limits in Table I

TABLE I:
FILTER DUTY LIMITS AS PER IEEE STANDARD 1036 – 1992

Duty	Limit, %
Peak Voltage	120
RMS Voltage	110
Peak Current	180
kVAr	135

V.PROBLEM DEFINITION

It is not a very practical distribution system but good from harmonic study point of view. The problem is defined as –

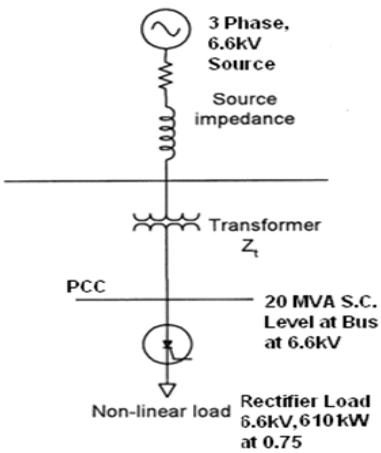


Fig 3: Single Line Diagram of the System

A six pulse converter operates from three phase 6.6 kV, 50 Hz, 650 kW at 0.75 power factor lagging. It is required to improve the power factor to 0.95 lagging. Short Circuit level is given as 20 MVA at PCC. Converter is the only load on PCC.

Harmonic data is given in Table-II

TABLE II.HARMONIC DATA

Harmonics	I_5	I_7	I_{11}	I_{13}	I_{17}	I_{19}
Current %	31	11	8	3	4	2

Fig. 3 shows the single line diagram of the system. 6.6 kV bus is the PCC. The short circuit MVA is given as 20 MVA at PCC. The power factor at PCC is 0.75. The active power drawn from the source is 650 kW. The rectifier rating is 610 kW.

VI.ANALYTICAL SOLUTION

Following steps are taken to obtain the analytical solution-

1)Reactive Power Compensation

The power factor is required to improve from 0.75 to 0.95. kVAr drawn by the converter before application of filter is 570 kVAr. kVAr drawn by the converter after application of filter is 214 kVAr. Total kVAr to be supplied by the filter is the difference between kVAr requirement before and after application of filter = 570 – 214 = 360 kVAr The reactive power can be distributed in the filter elements i.e. 5^{th} , 7^{th} and high pass filter branches as

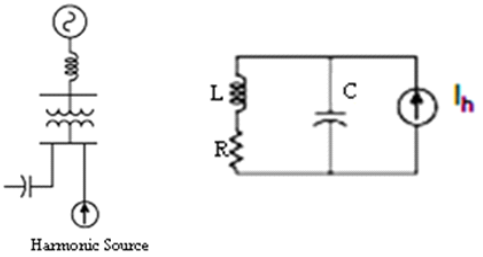
TABLE III
INITIAL THREE PHASE KVAR RATING OF EACH FILTER

Filter Type	kVAr rating
5th Single Tuned	120 kVAr
7th Single Tuned	120 kVAr
High pass	120 kVAr

1. 1:1:1 i. e. equally
2. 3:2:1

Tuned filters are subjected to less dielectric stress as compared to high pass filters. kVAr rating of high pass filter should be minimum to reduce the dielectric loss in it.

Choosing 1:1:1 i.e equal distribution of reactive power in all filter branches. Table III shows the filter rating.



(a) (b)

Fig 5 : (a) Single line diagram of system with capacitor bank (b) Equivalent circuit

DOI: 01.IJEPE.02.01.25

2)Calculation of Short-Circuit Level and Load Demand at PCC

To calculate the permissible TDD, the short-circuit level at the PCC and the load demand over a period of 15 or 30 min is required [8]. For this example, the 6.6-kV bus is PCC. The three phase symmetrical short circuit current I_{SC} is calculated as 3.03 kA. The maximum load demand current I_r is 80 Amps. The ratio $\frac{I_{SC}}{I_r}$ comes as 37.8. The permissible IEEE TDD distortion limits is 8.

3)Harmonic analysis without capacitor banks Following steps are taken to find out the voltage and current distortion factors.

a) The current distortion is found out by modeling the system represented in Fig. 2 in MATLAB® / SIMULINK.The current distortions are given in Table IV.
b) The system is represented by Norton's equivalent circuit shown in Fig. 5; A current source in parallel with the source impedance as viewed from the terminals of non-linear load.
c) The source impedance is recalculated at each harmonic frequency
d) As the harmonic currents are known, the bus harmonic voltages can be calculated, by IZ multiplication

4)Harmonic analysis with capacitor banks

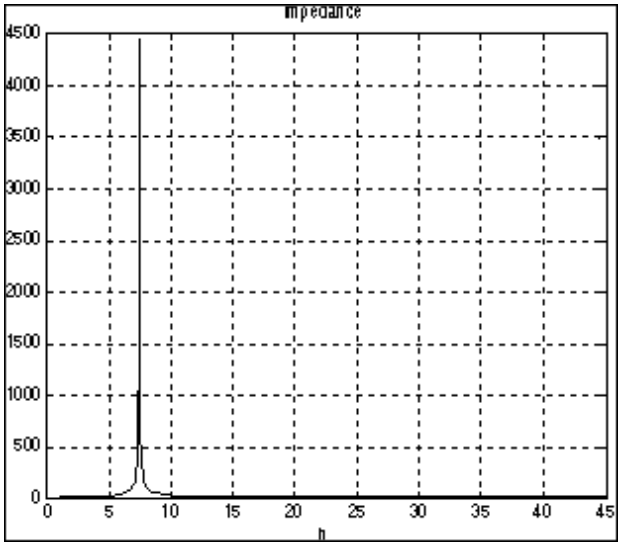


Fig 4 **:** Impedance modulus showing resonance at h = 7.44 harmonic with addition of 120 kVAr capacitor bank.

Estimation of resonance with capacitors

The parallel resonant frequency can be estimated as

$$h = \frac{kVAsc}{kVAr} \qquad (20)$$

where kVA_{SC} is the short circuit kVA rating at the PCC and kVAr is the capacitor kVAr rating. The parallel resonance frequency comes as 7.45. Fig 4 shows the impedance modulus of system. The parallel resonance occurs at the frequency of nearly 370 Hz.

Table V shows the harmonic loading of filter bank. It is seen that the 7th harmonic current is amplified due to parallel resonance present.The harmonic loading on the capacitor banks is calculated using Eq. (13) as 80.05 A capacitor current is 31.5 A and rms Current in capacitors is 80.05 A. The permissible rms current in the capacitors including harmonics is 1.8 times the rated current. The current loading is exceeded

The voltage loading is 4020 V, Vrms rated is 3810 V, Vrms permissible is 110% i.e. 4191 V. The voltage rating is not exceeded. The kVAr loading is calculated from Eq. (15) and is 212.2 kVAr / phase. The rated kVAr per phase is 120 kVAr and the limit is 135%. The kVAr loading is exceeded**.** Overall TDD is 110.2%. The harmonic voltage distortion is 33.5% . The total harmonic current demand distortion factor is 110.2%. Overall TDD for this system should not exceed 8%.

5)5th Harmonic Filter Design

Initial capacitor rating selected is 37.5 kVAr / phase at 3.81 kV / phase in star connection. The harmonic voltage distortion at PCC is 7.72% . TDD comes as 15%. Total TDD for this system should not exceed 8%.

TABLE IV
HARMONIC CURRENT FLOW AND HARMONIC VOLTAGE AT PCC

h	Harmonic Current Injected in PCC (A)	Harmonic Voltage V_h (V)	TDD	TDD Limits
5	24.37	252.1	30.46	7
7	9.28	138.58	11.6	7
11	9.05	214.9	11.31	3.5
13	3.87	113.25	4.84	3.5
17	4.93	189.57	6.16	2.5
19	2.02	86.9	2.53	2.5

TDD for 5th Harmonic is reduced to 2.0 as on limit of 7.0. But overall TDD exceeds the limit. Therefore selecting higher capacitor rating 85 kVAr, 4.16 Kv /phase . Capacitive reactance at power frequency is 203.59 &!. The filter reactor size is selected to tune the capacitor to the desired frequency of 250 Hz i.e. h = 5. The inductive reactance at power frequency is 8.14 &!.

Effective reactance of Filter X_{eff} is 195.45 &!. Effective three phase reactive power provided by the filter is 265.7 kVAr (3 phase rating). The harmonic voltage distortion at PCC is 6.81%

DOI: 01.IJEPE.02.01.25

TABLE V
HARMONIC CURRENT FLOW AND HARMONIC VOLTAGE AT PCC WITH CAPACITOR BANK

h	Harmonic Current Injected (A)	Current at PCC (A)	Current in the capacitor bank (A)	Harmonic Voltage at PCC (V)	TDD
1	-	-	31.5	3810	-
5	24.37	42.09	18.94	458.4	52.61
7	9.28	77.03	67.94	1174.5	**96.29**
11	9.05	7.61	16.58	182.4	9.51
13	3.87	1.95	5.96	55.5	2.44
17	4.93	1.21	6.34	45.1	1.51
19	2.02	0.38	2.48	15.8	0.48

TDD comes as 13.06 %. TDD for 5th Harmonic is reduced to 1.13 as on limit of 7.0. To reduce overall TDD within limit it is necessary to have a 7th harmonic filter.

6)7th Harmonic filter Design

The capacitor rating of 7th harmonic filter is 30 kVAr / phase and 4.16 V/phase. Capacitive reactance at power frequency is 576.85 &!.

The filter reactor size is selected to tune the capacitor to the desired frequency of 350 Hz. The inductive reactance at power frequency is $1.77\ \Omega$. Effective reactance of Filter $X_{eff} = 565\ \Omega$. Effective three phase reactive power provided by the filter is $Q_{eff} = 77.08\ kVAr$ (3 phase rating)

The harmonic voltage distortion at PCC is reduced to 5.04%. Overall TDD comes as 8.4%. TDD for 5th Harmonic is reduced to 0.64 as on limit of 7.0. TDD for 17th harmonic is 3.85 as on limit of 3.0 and 19th harmonics is 3.0 as on limit of 2.5. It shows necessary of high pass filter to limit the higher harmonics TDD. 7) High Pass Harmonic filter Design.Capacitor Rating is selected as 30 kVAr, 4.16 kV , $X_c = 572\ \Omega$ / phase.Tuning frequency f_0 = 11 and Quality factor of filter Q as 11.5. Resistor rating: 602.85 &! and Reactor rating: 0.0152 H, 4.16 kV / phaseThe harmonic voltage distortion at PCC is 2.67 % .Overall TDD comes as 4%.

TABLE VI
HARMONIC CURRENT FLOW AND HARMONIC VOLTAGE AT PCC WITH 5TH, 7TH AND HIGHPASS FILTER BANK

Analytical Calculation Results					Simulation Results				
Current at PCC (A)	Current in the 5th Harmonic filter capacitor bank (A)	Current in the7th Harmonic filter capacitor bank	Current in the HP harmonic filter capacitor bank (A)	TDD	Current at PCC (A)	Current in the 5th Harmonic filter capacitor bank (A)	Current in the7th Harmonic filter capacitor bank	Current in the HP harmonic filter capacitor bank (A)	TDD
-	19.49	6.74	6.66		-	23.18	6.73	6.65	-
0.76	24.19	0.1743	0.09	0.95	0.7	22.81	0.15	0.09	0.88
0.51	0.33	9.4032	0.16	0.64	0.61	0.39	11.06	0.19	0.76
1.66	0.67	1.6922	8.75	2.07	1.75	0.7	0.55	9.19	2.19
1.27	0.48	0.6619	1.99	1.59	2.21	0.83	0.57	3.41	2.76
2.06	0.72	0.7115	1.63	2.58	2.77	0.97	0.62	2.17	3.46
0.96	0.33	0.3065	0.67	1.2	1.79	0.61	0.4	1.23	2.24

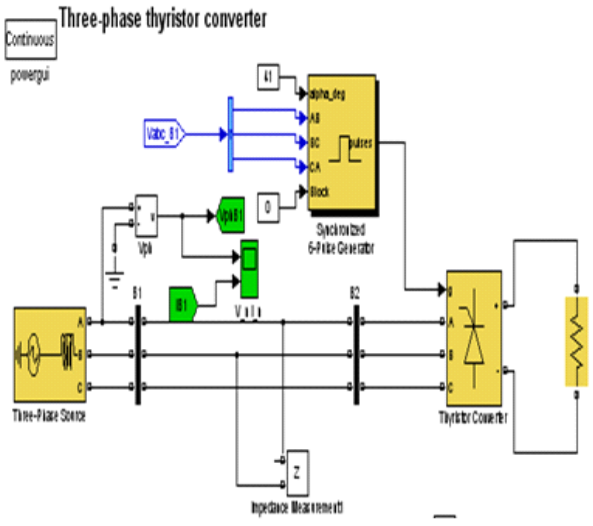


Fig 6 : SIMULINK model of the system

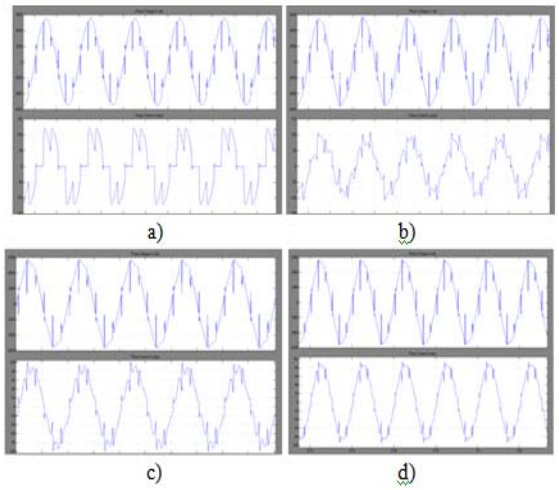


Fig.7: simulation results of distortions present in phase voltage and phase currenta) without Harmonic Filter. b) With 5th harmonic Filter c) With 5th and 7th harmonic Filter d) With 5th , 7th and high pass Filter.

DOI: 01.IJEPE.02.01.25

The analytical solution obtained for the TDD is compared with the simulation results in Table VI.

7) Effective Reactive power provided by filter and net power factor improvement

Finally the effective reactive power contribution of each star connected filter at fundamental frequency is

- 5th ST Filter - 265.7 kVAr
- 7th ST Filter – 77 kVAr
- HP Filter - 75 kVAr

Total compensation provided is - 417.7 kVAr. Net Power Factor improvement after installation of filter will be 0.99 i.e. near unity.

VII. Simulation of System and simulation results

The single line diagram of the system is simulated using MATLAB®/SIMULINK - platform to study the distortions in the voltage and current waveforms due to presence of nonlinear load in the system .The actual system can be modeled with a high degree of accuracy in this package. It provides a user interactive platform and a wide variety of numerical algorithms.

Fig. 6 shows the system modeled in SIMULINK. The system consists of six pulse Rectifier model as the nonlinear load to the system, gate signal generator block and three phase source.

Fig. 7 shows simulation results of distortions present in phase voltage and phase currents with and without filter assembly.

The comparison of simulation and analytical results is as follows-

1)With installation of 5th harmonic filter assembly:

A. Analytical calculation

- Overall TDD reduction to 13.88 % from 35.5%.
- The voltage distortion factor is reduced from 11.3 % to 6.75%.

B. Simulation results show that The overall TDD is reduced to 14.8 % from 35.5%.

2) With installation of 5th and 7th harmonic filters:

A. Analytical calculation - Overall TDD is reduced to 8.4% from 35.5%.

- The voltage distortion factor is reduced from 11.3% to 5.04%.

B. Simulation results

- The overall TDD is reduced to 10.55 % from 35.5 %.
- The voltage distortion factor is reduced from 11.3% to 6.4 %.
- The 7th harmonic current TDD is reduced to 0.64 from 11.6 analytically and simulation shows the reduction to 0.9.

3) After installation of high pass filter

A. analytical calculation shows that the overall TDD is reduced to 4% from 35.5%. The voltage distortion factor is reduced from 11.3 % to 3 %.

B. Simulation results shows that the overall TDD is reduced to 5.5 % from 35.5 %.The voltage distortion factor is reduced from 11.3% to 4%.

Thus, the TDD at PCC is within the limit specified by IEEE standard 519 -1992.[9]

VIII. CONCLUSION

This paper has presented a harmonic mitigation study in the simple distribution system. An investigation has been carried out to examine the effectiveness of filters using the two types of passive filters namely, single tuned and High pass filters in eliminating harmonics.

References

[1] Subrata De, and G. Bhuvaneswari, “Investigations on the impact of VAR rating and quality factor on the effectiveness of a shunt passive filter,” 0-7803-9525-5/06J. 2006 IEEE.

[2] J. C. Das, “Power System Analysis-Short-circuit, Load Flow and Harmonics”. New York: Marcel Dekker, 2002.

[3] J. Arrillaga, D. A. Bradley, and P. S. Bodger, “Power System Harmonics” New York: Wiley, 1985

[4] D. A. Gonzalez and J. C. McCall, “Design of filters to reduce harmonic
distortion in industrial power systems,” IEEE Trans. Ind. Applicat., vol.
IA-23, pp. 504–512, May/June 1987

[5] J. C. Das,” Passive Filter Potentialities and Limitations” IEEE Transactions on Industry Applications, Vol 40, No.. 1, Jan / Feb 2004

[6] Dugan, E.C., McGranagham, M.F., Santoso, **S.,** Beaty, H.W., “Elecirical power systems quality”**,** McGraw-Hill, 2002

[7] IEEE Standard for Shunt Power Capacitors. IEEE Standard 18- 1992

[8] “IEEE Guide for Application and Specification of Harmonic Filters”, IEEE Std. 1531-2003

[9] Recommended Practice and Requirements for Harmonic Control in Electrical Systems, IEEE Std. 519-1992.

DOI: 01.IJEPE.02.01.25